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A CMOS Inverter-based Approach to Exponential Pulse Generation

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A CMOS Inverter-based Approach to Exponential Pulse Generation

by

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A CMOS Inverter-based Approach to Exponential Pulse Generation

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The growing complexity of electrical systems has led to an increasing amount of wiring needed for many of these systems. For instance, in modern cars, the total length of electrical wiring easily exceeds 1 kilometer. Therefore, fast and accurate ways of testing for wiring faults become necessary. One way to detect a wiring fault is with time domain reflectometry, where fault locations can be detected by observing the reflections of an input pulse. However, due to dispersive effects, the pulse shape and speed will change while propagating down the line. Therefore, the choice of pulse shape is important in achieving high accuracy.

In this thesis, we present a CMOS inverter-based circuit for generating a pulse with an exponential leading edge. The key property of the exponential

function is that it stays exponential when differentiated or integrated. In that way, dispersion can be minimized. Additionally, as process, voltage and temperature (PVT) present reliability issues in practical design, we also present circuits that are used to stabilize critical parameters.

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Chapter 1

Introduction

1.1 Overview

As electronic systems age over time, faults in their wiring become increasingly common. Eventually, catastrophic failure may occur if these faults go undetected. This is especially important to prevent in systems such as aircraft and cars, as failure in their electronic systems may result in human casualties. Additionally, there is a heavy maintenance cost in repairing wires. For instance, it is estimated that between 1 million and 2 million man-hours are needed to detect and repair faulty wiring in the U.S. Navy alone [5]. Additionally, replacement of the wiring system in a typical aircraft may cost anywhere from $1 - 7 million [3]. Clearly, there is a need for an accurate and fast detection mechanism for wiring faults, to minimize cost and time spent repairing these faults.

One way to detect wiring faults is time domain reflectometry (TDR). A narrow pulse is sent down a wire, which will reflect if any fault or impedance

discontinuity is encountered [14]. The time interval between the incident and reflected signal can be used to locate the wire fault. A popular choice of pulse shape is the square wave, but the accuracy of fault detection is limited by the dispersion of the propagating pulse [8]. We propose that a pulse with a leading exponential edge minimizes dispersion, because all derivatives and integrals of the exponential function map onto the exponential.

Additionally, as CMOS scaling trends continue, new analog circuit design techniques become necessary. For instance, as power supply voltages are lowered due to digital power constraints, headroom issues arise in analog circuits, limiting the ability to gain boost via cascoding [9]. Similarly, shorter channel lengths result in an increase in output conductance, lowering the intrinsic device gain. Therefore, in this thesis we explore the viability of using a CMOS inverter as an amplifier, over the more traditional operational amplifier (opamp). Additionally, the inverter provides flexibility in re-use, low area, and low power consumption.

1.2 Prior Art

Circuits for exponential pulse generation have been previously proposed. This section introduces some previous circuit designs, and the methods used to generate the exponential waveform.

1.2.1 BJT Based Design

One natural way of of producing an exponential pulse is to take advantage of the I-V characteristics in a bipolar junction transistor (BJT) [13]. In this design, special care is taken to make the final output robust to PVT. Figure

1.1 shows the full circuit diagram.

The transistor Q_1 provides the exponential current, which is converted to an output voltage through R_1. An offset generator is needed to replace the temperature dependent, reverse saturation current I_S with a temperature independent current I_o. A PTAT current generator, combined with a ramp generator, is used to to make the input voltage PTAT. That way, $e^{\frac{v(t)}{V_T}}$ is independent of temperature.

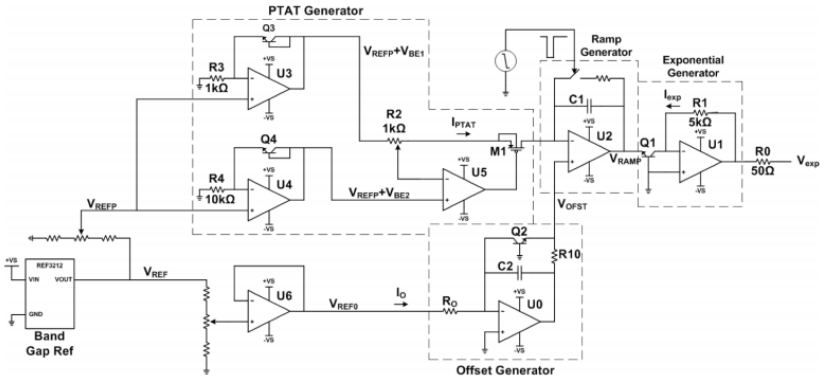

Figure 1.1: BJT based exponential pulse generator, as described in [13].

1.2.2 2^{nd} Order Power Series Based Design

A CMOS circuit that produces a current with exponential characteristics is presented [2]. Because MOS transistors are square law devices, a reasonable approximation to an exponential function can be made by computing the series expansion, up to the second order term.

Figure 1.2 shows the proposed circuit. The devices M_3, M_4, M_8, and M_9 form two current mirrors. The drain currents I_{d1}, I_{d4}, and I_{d9} are all equal, so no current flows from the source of M_1 to the gate of M_2. Transistors M_6

and M_7 will force the node V_a to half V_{SS}, if M_6 and M_7 are sized identically. Then, the output current can be given as the sum of the drain currents of M_2 and M_5. Assuming they operate in the saturation region with no body effect, then I_{out} can be written as

$$I_{out} = K_n(\frac{-V_{SS}}{2} - V_{th,n})^2\left(1 + \frac{V_{in}}{\frac{-V_{SS}}{2} - V_{th,n}} + \frac{V_{in}^2}{2(\frac{-V_{SS}}{2} - V_{th,n})^2}\right) \tag{1.1}$$

$$K_n = \mu_n C_{ox}\frac{W}{L} \tag{1.2}$$

We find from this equation that an input voltage generates an output current, with a constant term, a term that varies linearly with V_{in}, and a term that varies as the square of V_{in}. However, from equation 1.1 it is clear that I_{out} will vary substantially with PVT, due to a strong dependence on terms such as K_n and V_{th}. Therefore, we take a different design approach in this thesis, where the basic building block is an inverter, not a single transistor. This inverter is then stabilized using a replica inverter, making the design more robust against PVT.

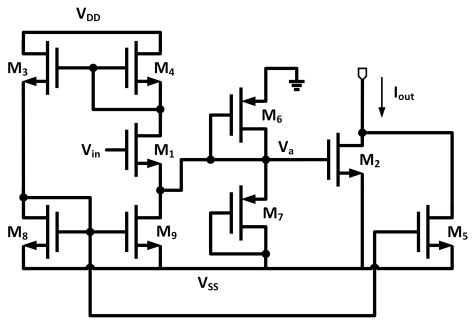

Figure 1.2: CMOS circuit with exponential V-I conversion, as proposed in [2].

1.3 Organization

This thesis is organized as follows. In chapter 2, the mechanism for generating an exponential pulse is described. Additionally, we discuss the differences between the traditional opamp-based integrator, and the implemented inverter-based integrator. Chapter 3 describes a first design of the exponential pulse generator, along with techniques used to stabilize critical device parameters. The layout of the different circuit blocks are shown, along with post-layout simulations. Finally, we describe the testbench setup and measurement results of the taped out chip. Chapter 4 describes a second design of the same exponential pulse generator, this time with a much shorter pulse duration. Simulation results are presented as well. Chapter 5 summarizes the work done, and provides some ideas for future work.

Chapter 2

Background

2.1 Principle of Operation

This section describes the method that we use to generate an exponential pulse. We first describe the series expansion of the exponential function, while providing some insight into the accuracy of this approach. Then, we will introduce a method to build up the exponential pulse using integrators and summers. Additionally, we analyze both large and small signal characteristics of an inverter acting as an amplifier. Finally, the inverter-based integrator approach used in this system is compared to a traditional integrator.

2.1.1 The Exponential Function

The exponential function can be defined as a power series

$$e^x = \sum_{k=1}^{\infty} \frac{x^k}{k!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + ... \tag{2.1}$$

From this expression, we see that each term after the first can be generated by integrating the previous term. Therefore, we can re-write e^x as a summation of integrals

$$e^x = 1 + \int 1dx + \int\int 1dxdx + \int\int\int 1dxdxdx + ... \tag{2.2}$$

where the exponential function can be built up through a cascaded network of integrators and summers, as depicted in figure 2.1.

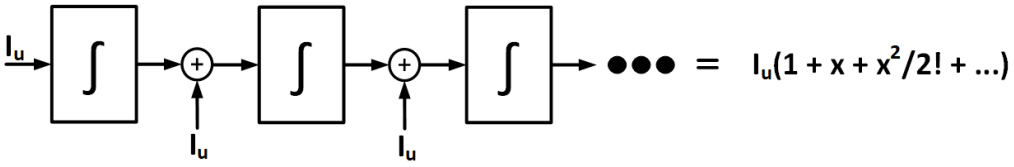

Figure 2.1: Integrator Chain.

Figure 2.1 shows that a unit value, in this case I_u, is initially integrated, then continually accumulated at the start of the succeeding integrator inputs.

As more stages are added, the final expression converges to an ideal exponential, but with diminishing returns. For instance, if I_u and x are set to 1, then the sixth term is $\frac{1}{120}$, which constitutes less than 1% the value of e ($\approx$ 2.72). As each integration stage is realized by the same non-ideal integrator, we decide to limit the number of integration stages to 5. Additionally, since every higher order integration stage requires the same amount of power consumption as the lower order stages, power dissipation increases with each stage added.

2.2 The Inverter

Consider a typical CMOS inverter as shown in Figure 2.2. V_{LT} is defined as the voltage at which both input and output terminals are at the same value, that is $V_{in} = V_{LT}$ [11]. Then, the currents I_{Mp} and I_{Mn} are equal. This value of V_{LT} is usually close to $\frac{V_{DD}}{2}$, depending on the relative sizing of the NMOS and PMOS devices.

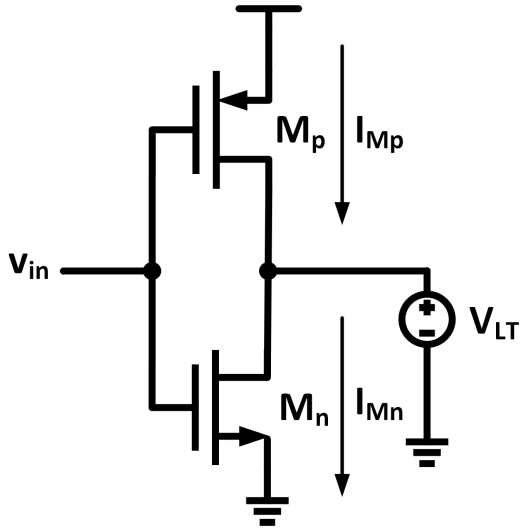

Figure 2.2: Inverter with output voltage held at V_{LT}.

2.2.1 DC Characteristics

As the input voltage is swept from 0 to V_{DD}, the output transfer characteristics are plotted in figure 2.3. If we assume that the PMOS device is around 2-3x as wide as the NMOS, then the V_{LT} will lie about halfway from 0 to V_{DD}. This sizing difference is to account for the mobility difference between holes and electrons. In this situation, both NMOS and PMOS devices are in saturation

region and the inverter is operating in the high gain region. As shown in the figure, this region is where the slope is the highest. The derivative of the curve near V_{LT} is the small-signal gain of the inverter, and a high gain is necessary to build an integrator using inverters.

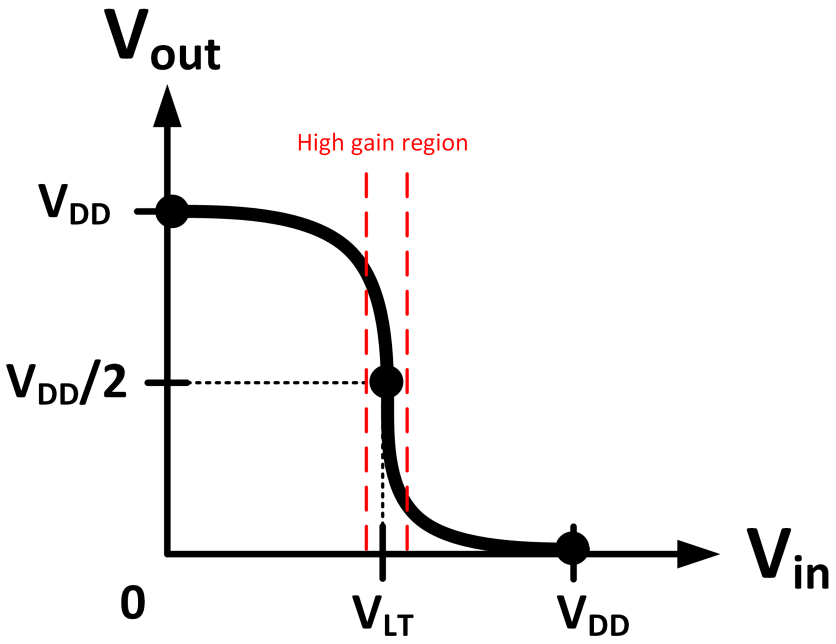

Figure 2.3: Large signal transfer characteristics of an inverter.

2.2.2 AC Characteristics

If both the NMOS and PMOS devices of an inverter are in saturation, then the inverter acts as an amplifier with large small-signal gain. Figure 2.4 shows a circuit diagram of the small-signal model of the inverter. The transconductances of the NMOS and PMOS devices are denoted as g_{m1} and g_{m2}, respectively. Similarly, output resistances are denoted as r_{o1} and r_{o2}.

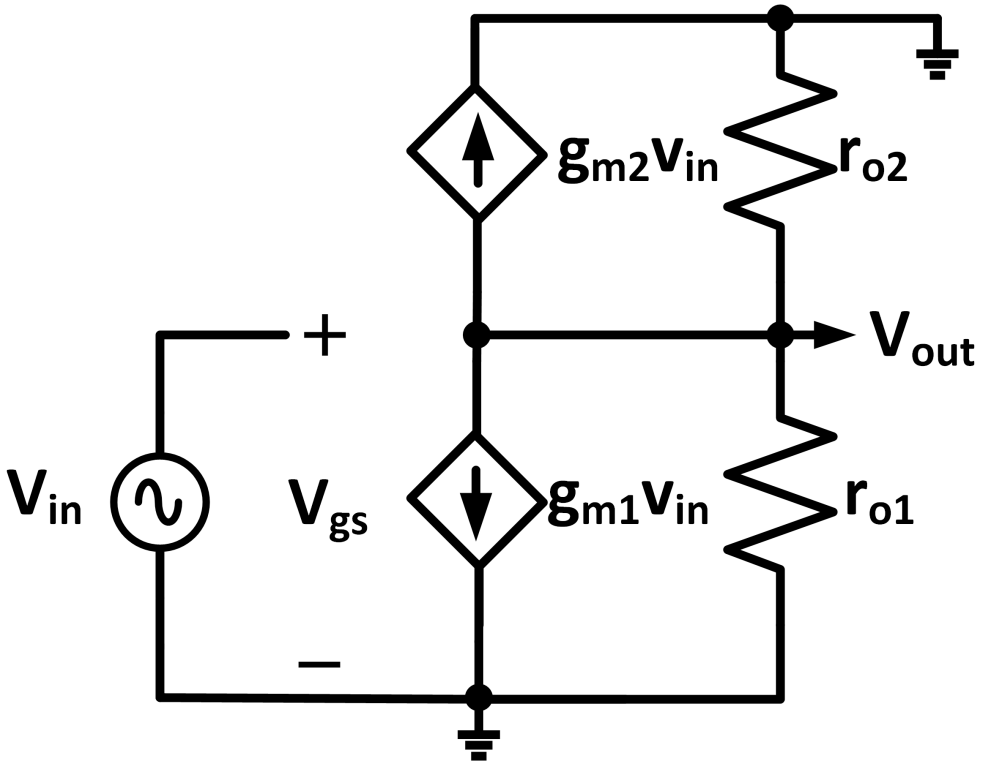

Figure 2.4: Small-signal model of an inverter amplifier.

From figure 2.4 we can calculate the gain as

$$\frac{v_{out}}{v_{in}} = -(g_{m1} + g_{m2})(r_{o1}||r_{o2}) \tag{2.3}$$

We show in a later section that the value of this gain affects the integrator output. In addition, in the limit as overall g_m (g_{m1} + g_{m2}) gets large, the integrator itself becomes more ideal.

2.3 The Integrator

An integrator is any circuit that performs the mathematical operation of integration, where the output voltage is proportional to the integral of the input voltage. Typically, the act of integration is done through the accumulation of charge on an integrating capacitor. This section begins by introducing a typical op-amp based integrator, and continues by describing the core circuit of this thesis, which is the inverter-based integrator.

2.3.1 Op-amp Based Integrator

Figure 2.5 shows a typical op-amp based integrator. Assuming an ideal op-amp, we can apply Kirchhoff's current law to node V_n and write

$$\frac{V_{in}}{R} = -C\frac{d(V_{out})}{dt} \tag{2.4}$$

knowing that the current - voltage relationship in a capacitor is

$$I = C\frac{dv}{dt} \tag{2.5}$$

since V_n of an ideal op-amp is 0. Integrating with respect to time results in

$$V_{out} = -\frac{1}{RC}\int_0^t V_{in}dt \tag{2.6}$$

In this integrator, the input voltage in series with the resistor R generates a current, and since the node V_n acts as virtual ground, all the current is fed into the feedback capacitor. The capacitor charges at the rate determined by

the time constant τ, which is simply

$$\tau = RC \tag{2.7}$$

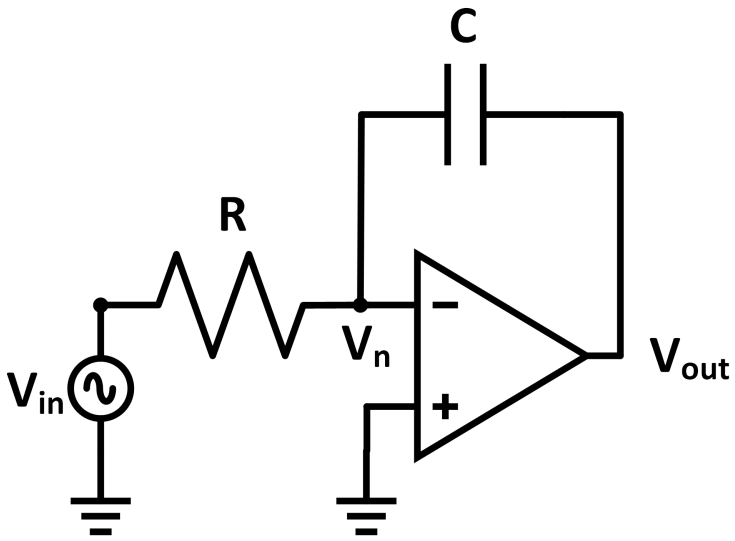

Figure 2.5: Op-amp based integrator.

2.3.2 Inverter-based Integrator

An inverter-based integrator is similar to the typical op-amp based integrator, with a few key differences. First, the inverter does not have a virtual ground node as in the case of the op-amp. Secondly, a g_m stage is used instead of a resistor. This serves the purpose of converting the voltage at the output of the integrator back into a current for use in the next stage.

Figure 2.6 shows the circuit diagram of the inverter-based integrator. For the purposes of distinguishing the two inverters in a single integrating block, each inverter with a feedback capacitor will be called the integrating

inverter, and the ones acting as a transconductance stage will be referred to as the g_m inverter. The switch S is used to periodically reset the integrating capacitor, thereby resetting the exponential pulse. The frequency at which this happens depends on how fast the pulse rises. Right before the pulse reaches an amplitude which would drive device M2 into triode region, the switch will close, resetting the capacitor.

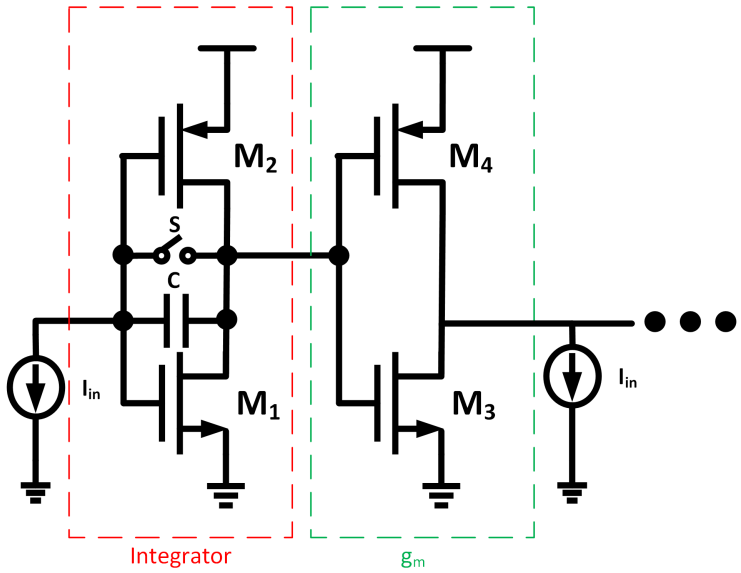

Figure 2.6: The inverter-based integrator. The circuit highlighted in red is the integrator, and the circuit in green converts the integrator output back into a current, which is then summed into the next stage.

Figure 2.7 shows the equivalent circuit model for the inverter-based integrator. The integrator is represented as a voltage amplifier with gain A, with a output resistance r_o in series. The g_m stage is represented by a standard voltage controlled current source. Writing the KVL around the first loop and solving

for v_{out} we obtain

$$v_{out} = \frac{A}{1+A}\frac{I_{in}}{C}t - \frac{I_{in}r_o}{1+A} \tag{2.8}$$

Therefore the integration of a constant current I_{in} produces a voltage ramp at the output, but first there will be a negative jump due to the $\frac{I_{in}r_o}{1+A}$ term. For a sufficiently large A, then $\frac{A}{1+A} \approx 1$ and the slope of the ramp is determined by I_{in} and C. The integrator output voltage converts into a current sink by the inverter acting as a g_m stage, which is integrated in the next stage.

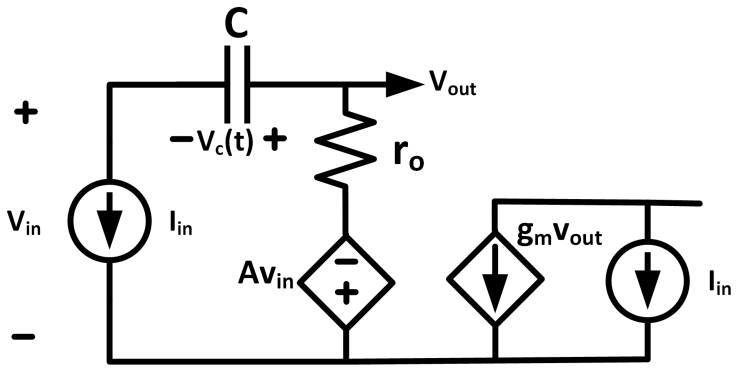

Figure 2.7: inverter-based integrator equivalent circuit. The output resistance of the inverter is given as r_o and the gain as A.

The output current due to the g_m stage is

$$I_{out} = I_{in}(\frac{A}{1+A}\frac{g_m}{C}t - \frac{g_m r_o}{1+A}) \tag{2.9}$$

with the time constant is given as

$$\tau = \frac{C}{g_m} \tag{2.10}$$

From equations 2.9 and 2.10 we can calculate the total current sink feeding the second stage as

$$I_{in,2} = I_{in}(1 + \frac{A}{1+A}\frac{t}{\tau} - \frac{g_m r_o}{1+A}) \tag{2.11}$$

This calculation then repeats, with $I_{in,2}$ being used as the new I_{in}. We can see from equation 2.10 that to get the fastest rising pulse, C needs to be minimized while the g_m needs to be maximized. Additionally, increasing the g_m of the integrator also has a benefit in minimizing the negative jump in magnitude, due to increasing A. Furthermore, the next section explains how increasing the integrator g_m causes the integrator to become more ideal.

2.3.3 Impact of Finite Integrator g_m

In any realizable system, the assumption of infinite g_m is often unrealistic. Therefore, it is of interest to determine the effects of finite g_m in the inverter-based integrator.

Figure 2.8 shows the small-signal equivalent model of the circuit in figure 2.6, with the transconductance stage preceding the integration stage. In this figure, g_{m1} refers to the transconductance of the g_m stage, and g_{m2} refers to the transconductance of the integrator stage, r_{o1} and r_{o2} are output impedances, and C_L is the load capacitance seen at the input of the next stage.

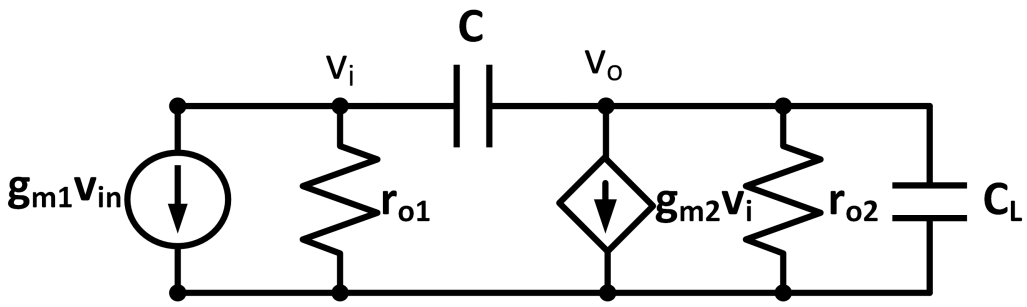

Figure 2.8: Small signal model of the inverter-based integrator.

We can write two KCL equations at nodes V_i and V_o as follows

$$g_{m1}v_{in} + \frac{v_i}{r_{o1}} + (v_i - v_o)sC = 0 \tag{2.12}$$

$$g_{m2}v_i + \frac{v_o}{r_{o2}} + v_o sC_L + (v_o - v_i)sC = 0 \tag{2.13}$$

Solving the two equations for the transfer function yields

$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{(\frac{sC+\frac{1}{r_{o2}}+sC_L}{(g_{m2}-sC)r_{o1}})(1+sC)+sC} \tag{2.14}$$

From equation 2.14, we can see the impact of g_{m2}. We can take the limit as g_{m2} approaches infinity and write

$$\lim_{g_{m2}\to\infty} \frac{v_o}{v_{in}} = \frac{g_{m1}}{sC} \tag{2.15}$$

recovering the ideal integrator transfer function.

Chapter 3

Exponential Pulse Generator: First Design

This chapter explores the complete, circuit level design of an exponential pulse generator. First, we will describe the sensitivity of an inverter to supply variations, and also present circuits that stabilize critical parameters such as g_m and V_{LT}. Then, we present the full, 5-stage exponential pulse generator schematic. Additionally, we present the layout of all the circuit blocks, and the post-layout simulations. Finally, we provide the testbench setup and measurement results.

3.1 Stabilizing g_m and V_{LT}

The transconductance (g_m) and logical threshold (V_{LT}) of an inverter vary strongly over PVT. This necessitates the use of circuits that can regulate these parameters, which will make the overall design more reliable. In this section, we first explore why inverters are PVT sensitive, and also present some circuits that solve this problem.

3.1.1 Effects of Supply Voltage Variation

As defined in Chapter 2, an inverter biased at V_{LT} has equal currents flowing through both NMOS and PMOS devices. Knowing that $I_{Dp} = I_{Dn}$, we can use the quadratic model of a MOSFET in saturation and write

$$k_n(V_{GS,n} - V_{th,n})^2 = k_p(V_{GS,p} - |V_{th,p}|)^2 \tag{3.1}$$

where

$$k = \frac{1}{2}\mu C_{ox}\frac{W}{L} \tag{3.2}$$

If $V_{in} = V_{LT}$, then re-arranging equation 3.1 leads to

$$V_{LT} = \frac{\sqrt{k_p}(V_{DD} - |V_{th,p}|) + \sqrt{k_n}V_{th,n}}{\sqrt{k_p} + \sqrt{k_n}} \tag{3.3}$$

From equation 3.3, we find that V_{LT} is strongly dependent on the supply voltage. Similarly, the g_m of the inverter is given in [16] as

$$g_m = \sqrt{k_p k_n}(V_{DD} - |V_{th,p}| - V_{th,n}) \tag{3.4}$$

Therefore, not only is V_{LT} a strong function of V_{DD}, but so is g_m. Furthermore, it is well known that mobility varies with temperature [4]. This will cause $k_{n,p}$ to vary accordingly. Additionally, differences in doping concentration, lithography, and other processes result in different process corners [18]. The differences in process corners can vary the V_{th} of a transistor by a large amount. An analysis of the effects of device parameter mismatch is given in [7, 10, 12]. In the next section, we present circuits that can be used to account for these variations.

3.1.2 Generating a Stable Supply Voltage

One way to account for process variations is to use replica biasing techniques [6, 15]. The main idea is to stabilize relevant circuit parameters by canceling out PVT dependencies through continual adjustment of bias voltages or currents.

We employed a technique that was presented in [16]. This technique generates a local power supply, V_{DDR}, that can be used to bias the integrating inverters. V_{DDR} is such that all inverters biased by it will have a well defined V_{LT}, derived from a reference voltage V_{REF}. This circuit is presented in figure 3.1.

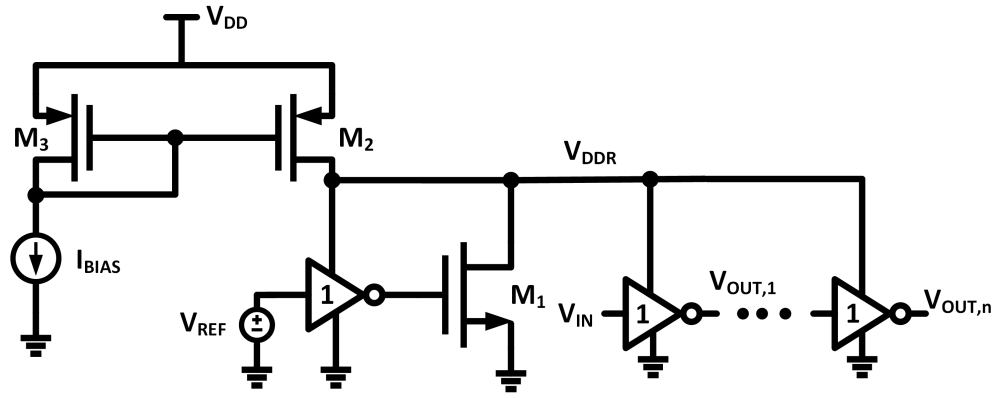

Figure 3.1: Circuit to generate V_{DDR}, as presented in [16].

In this circuit, a replica inverter with a voltage V_{REF} at the input generates a regulated voltage V_{DDR}, which takes on a value of about 2x V_{REF}. The NMOS device M_1 creates a negative feedback loop that keeps the V_{DDR} local supply relatively constant. The current mirror devices M_3 and M_2 are sized appropriately so that all inverters that are biased by V_{DDR} have adequate DC current. Each inverter biased by V_{DDR} is sized the same as the replica. Table

3.1 shows the device sizing. In the next section, we will discuss how to bias the g_m inverters.

Device	Size (μm)
M_1	0.3/1.5
M_2	24/0.5
M_3	4/0.5

Table 3.1: Transistor sizing for V_{DDR} generating circuit.

3.1.3 Stabilizing g_m

The technique for stabilizing g_m is similar to the technique presented in the previous section. A circuit, shown in figure 3.2, generates a supply $V_{DDR,gm}$, where inverters biased by it have a constant g_m [16].

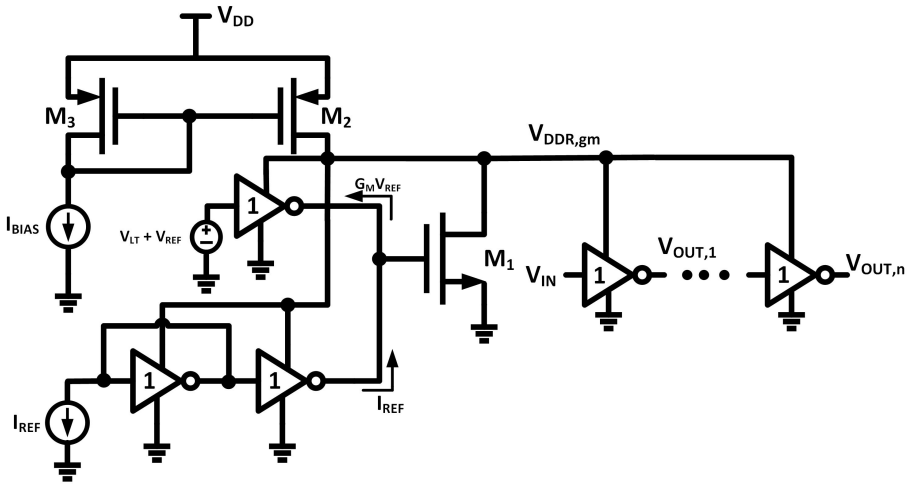

Figure 3.2: Circuit to generate V_{DDR}, as presented in [16].

A unit inverter biased by a voltage V_{LT}+V_{ref} sinks current equal to $g_m V_{ref}$. A current I_{ref} is passed through two inverters that form a current mirror, and $V_{DDR,gm}$ is adjusted so that KCL at the gate of M_1 is satisfied. This can be written as

$$g_m = \frac{I_{ref}}{V_{ref}} \tag{3.5}$$

As with the V_{LT} regulator circuit, transistor M_2 is sized properly so that all g_m inverters biased by $V_{DDR,gm}$ have adequate bias current. Table 3.2 shows the device sizing for this circuit.

Device	Size (μm)
M_1	0.3/0.4
M_2	24/0.6
M_3	4/0.6

Table 3.2: Transistor sizing for $V_{DDR,gm}$ generating circuit.

3.2 Full Schematic

With these auxiliary circuits in mind, we present the full schematic of the exponential pulse generator, shown in figure 3.3. The blocks labelled $V_{LT,REF}$ and $G_{M,REF}$ are the circuits described in 3.1.2 and 3.1.3.

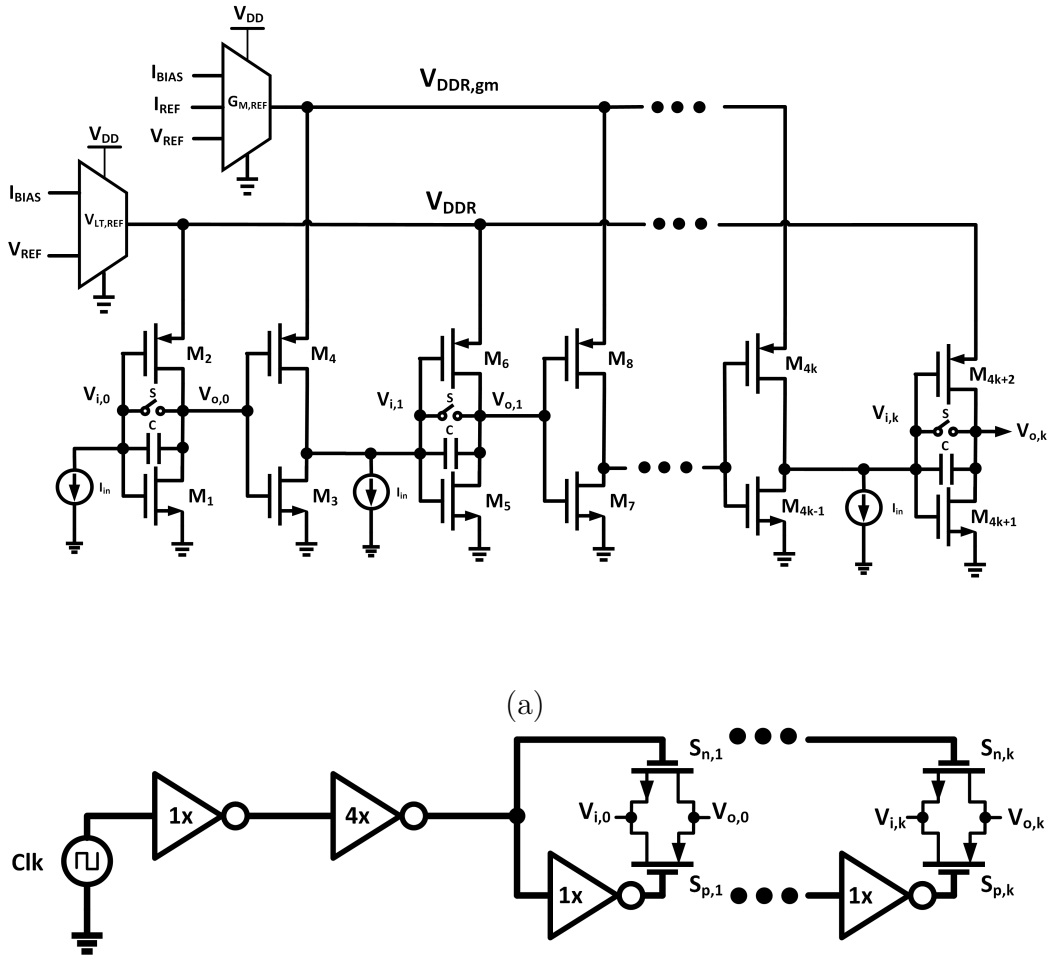

Figure 3.3: (a) Full exponential pulse generator schematic. (b) Clock drivers and implementation of switches.

As shown in the full schematic, the V_{LT} and g_m reference circuits are used to generate regulated supply voltages that bias the inverter chain. The integrators are biased with V_{DDR}, and the g_m inverters are biased with $V_{DDR,gm}$. There are a total of k+1 integration stages. For instance, k=4 means a 5 stage design.

The corresponding g_m stage for the last integrator is omitted, because we only need the voltage output of the integrator.

Additionally, a pair of NMOS/PMOS switches are used to implement the switches, as shown in figure 3.3 (b). This transmission gate structure is preferable to using a single NMOS or PMOS because it ensures the voltage at the input and output are equivalent. Then, the feedback capacitor can be discharged properly. Furthermore, an inverter chain of increasing size is used to buffer the input clock signal. This is to drive the large capacitance seen the gates of the switches, which increases as more stages and switches are added. These switches are implemented as medium V_{th} devices.

The unit currents are generated with a non-cascoded current mirror. Additionally, this mirror is also used to generate the I_{BIAS} shown in figures 3.1 and 3.2, and also the I_{REF} current in figure 3.2.

Device	Size (μm)
Integ. NMOS	0.9/5.5
Integ. PMOS	2.1/5.5
g_m NMOS	0.3/7
g_m PMOS	0.6/7

Device	Size
NMOS	0.6/0.3
PMOS	1.2/0.3

Table 3.3: (left) Sizings for integrator/g_m inverters. (right) Sizings for switch devices.

3.3 Layout

In this section, we present the layout of each circuit block. The figures below (3.4 - 3.8) show the layouts of each circuit block in the chip. There is an

additional output buffer included, as a low impedance output is needed to drive the substantial capacitance at the output.

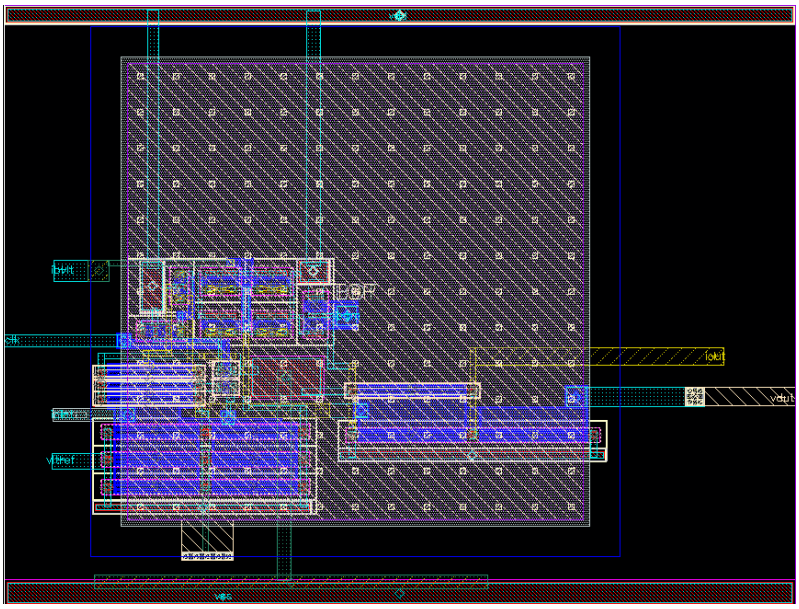

Figure 3.4: Single integrator and g_m stage. A large MIM capacitor is connected on metals 5 and 6.

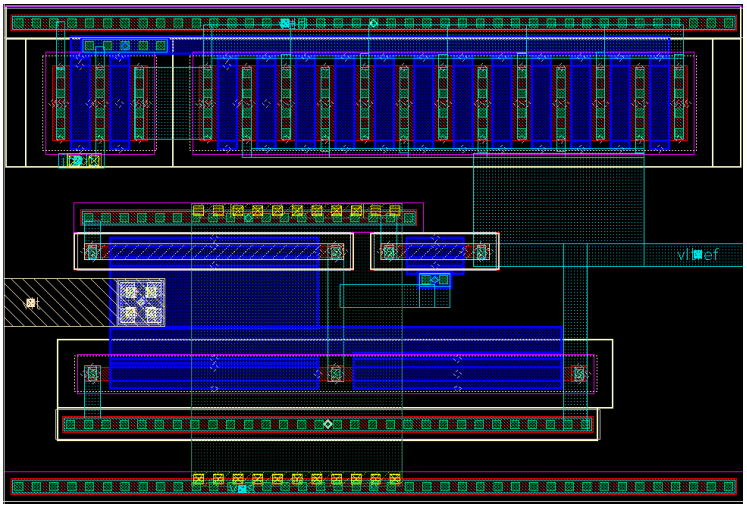

Figure 3.5: V_{LT} regulating circuit.

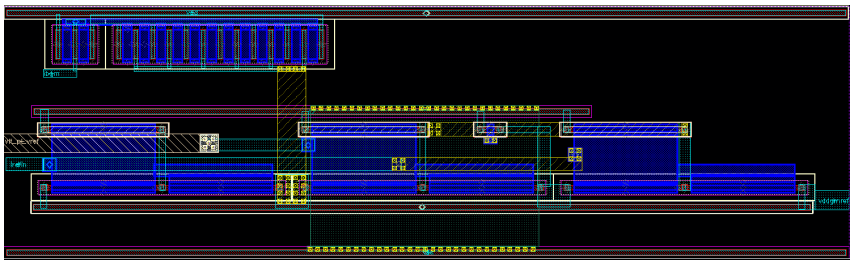

Figure 3.6: g_m regulating circuit.

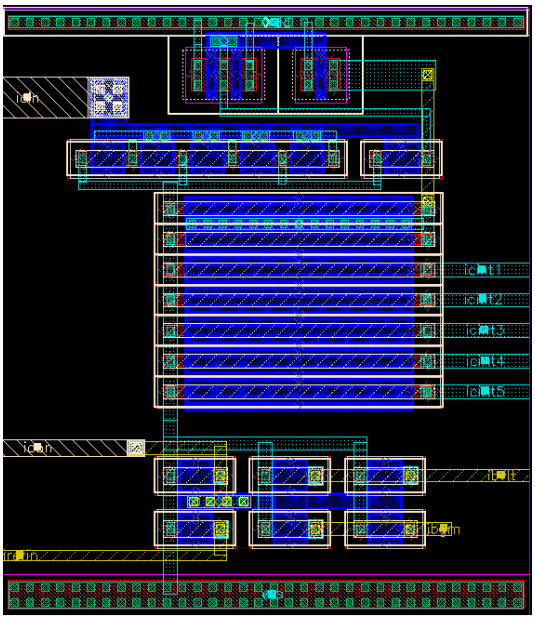

Figure 3.7: Current mirror. This version of the current mirror was not cascoded.

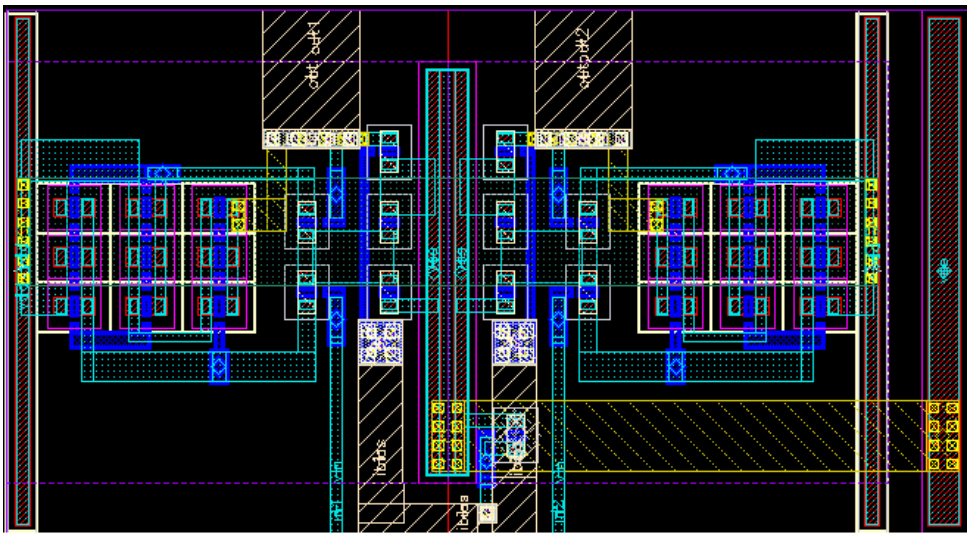

Figure 3.8: Output buffer used to drive pad capacitance.

3.4 Post-Layout Simulations

After layout, the exponential pulse generator is simulated with the extracted netlists. In this section, the post-layout simulations are presented. In particular, we plot the fifth stage output, along with the regulated voltages V_{DDR} and $V_{DDR,gm}$. This design targeted an integration time constant $\tau = 100$ ns, so after 500 ns the fifth stage output should rise to close to its peak value. Note that this spec is the same as the one used in the BJT-based design [13]. These plots will be shown at typical PVT, and also at different corners (SS,FF,SF,FS), three different supply voltages (1.62 V, 1.8 V, 1.98 V), and three different temperatures (0°C, 27°C, 100°C). For each plot, we keep either temperature or supply voltage fixed, and plot the outputs over different process corners. This way we can understand how temperature or supply voltage affects the output individually. A 5 pF output capacitor is added to act as

a load. This causes the discharge to fall much more slowly. First, a quick comparison between pre-layout and post-layout is done for the pulse at typical PVT. As shown in figure 3.9, the two pulses are quite similar. Therefore, we do not expect the layout to introduce any significant deviation in the design. Additionally, the pulse takes around 500 ns to reach its peak, which is what we designed it to do.

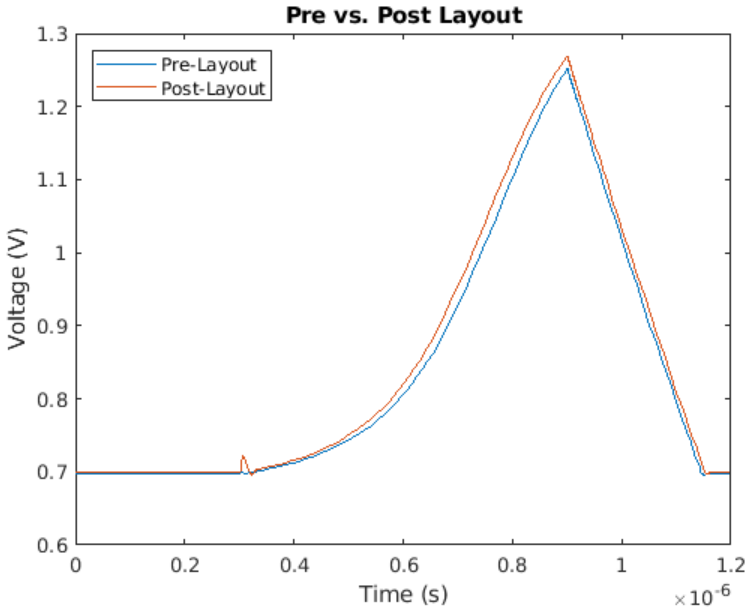

Figure 3.9: Pre-layout vs post-layout simulation.

3.4.1 Outputs Over PVT

Figure 3.10 below shows the pulse over PVT. In terms of temperature, the worst case scenario is given in the center right plot, where T=100°C. In this case, pulse looks substantially more linear. Considering supply voltage changes, we find that the pulse more closely resembles the typical case. This

is because the regulating circuits are able to provide stable reference voltages even though the supply changed.

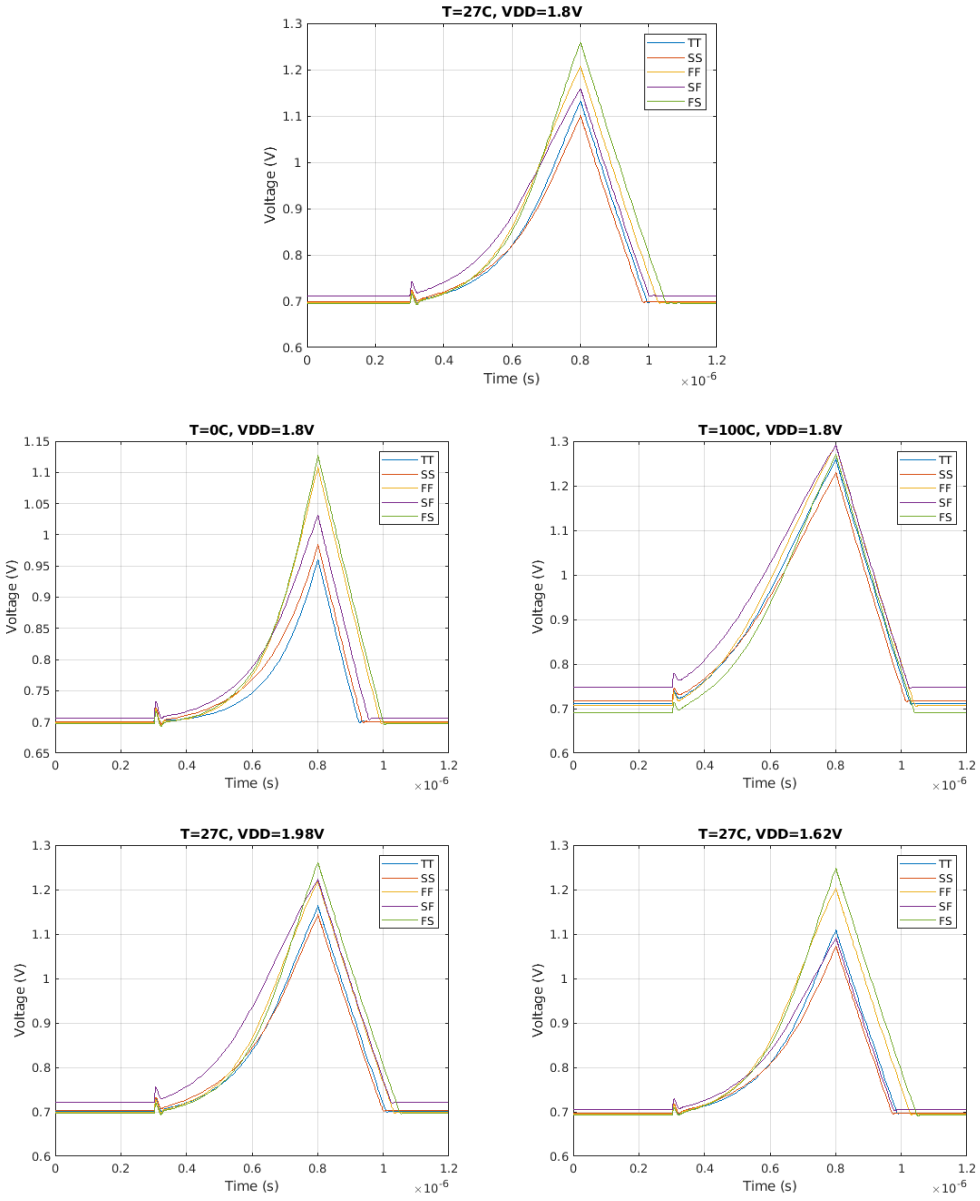

Figure 3.10: Variations in the exponential pulse due to PVT. The top center plot is at typical temperature and typical supply voltage. The middle and bottom plots are at low/high temperatures and supply voltages, respectively.

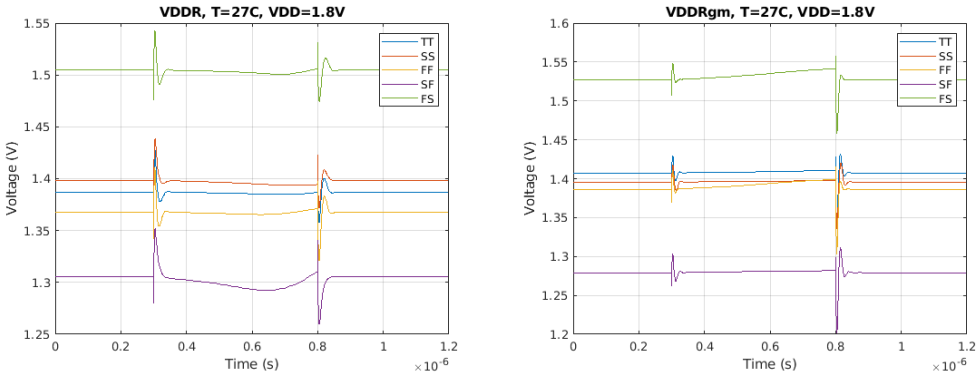

Figure 3.11: V_{DDR} and $V_{DDR,gm}$ at normal temperature and supply voltage.

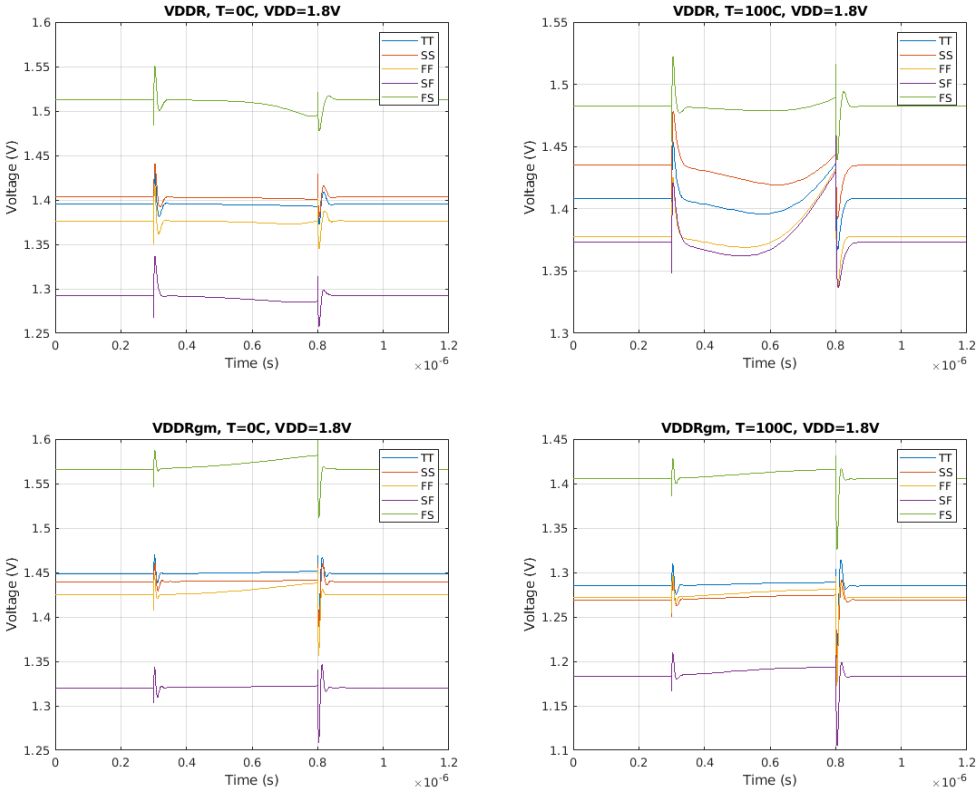

Figure 3.12: Effects of temperature variation on V_{DDR} and $V_{DDR,gm}$.

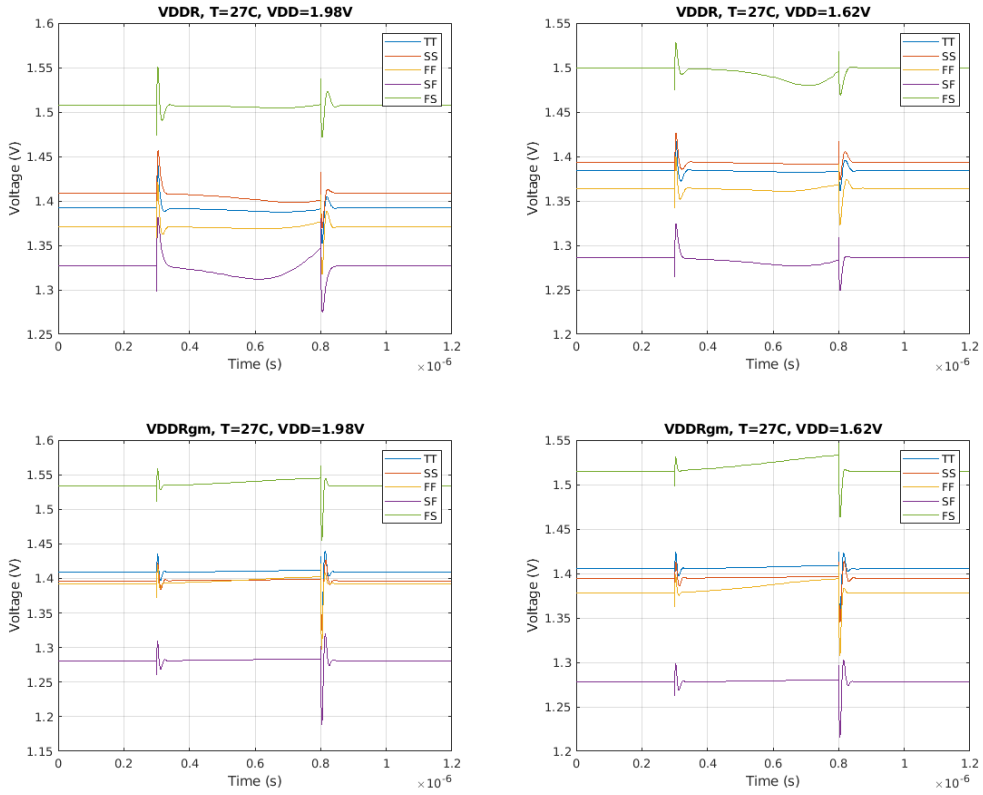

Figure 3.13: Effects of supply voltage variation on V_{DDR} and $V_{DDR,gm}$.

Both V_{DDR} and $V_{DDR,gm}$ are plotted over PVT. Figure 3.12 shows the effect of temperature variation, and figure 3.13 shows the effect of supply voltage variation. These two groups of plots are compared to figure 3.11, which shows the case where both temperature and V_{DD} are normal. As before, we find that the worst case for V_{DDR} is at T=100°C. As shown in the top right plot of figure 3.12, this is where the regulated voltages have the most variation during the integration time. With few exceptions, both references stay quite stable throughout the integration period.

3.5 Chip Testing

In this section, we discuss the testbench setup and measurement results. A breadboard was used to build the testbench, and testing was done in the undergraduate circuits labs at UT.

3.5.1 Testbench Setup

The chip was packaged using a TQFP44 package. A 44 pin socket was used to connect the chip onto a breadboard properly. In total, there are 7 inputs and 4 outputs, so not all pins were used. The breakdown of inputs and outputs are described in tables 3.4 and 3.5, respectively. All current inputs are generated by using by using a voltage source and appropriately sized resistor. A picture of the breadboard setup is given in figure 3.14.

Input	Description
$V_{DD,3.3}$	3.3 V supply to energize chip pad ring
$V_{DD,1.8}$	1.8 V circuit supply
V_{lt}	Used to supply V_{REF}, as in figure 3.2
V_{lt}_pl_V_{ref}	Used to supply V_{LT}+V_{REF}, as in figure 3.3
I_{cin}	Sets the bias current for the V_{LT} and g_m regulator circuits
I_{con}	Sets the integrating current for all integrators
I_{buf}	DC bias current for output buffer

Table 3.4: Inputs and their descriptions.

Output	Description
V_{DDR}	Same V_{DDR} as in figure 3.2
$V_{DDR,gm}$	Same $V_{DDR,gm}$ as in figure 3.3
$V_{out,1}$	Exponential pulse, output of the fifth integrator stage
$V_{out,2}$	Fourth stage output

Table 3.5: Outputs and their descriptions.

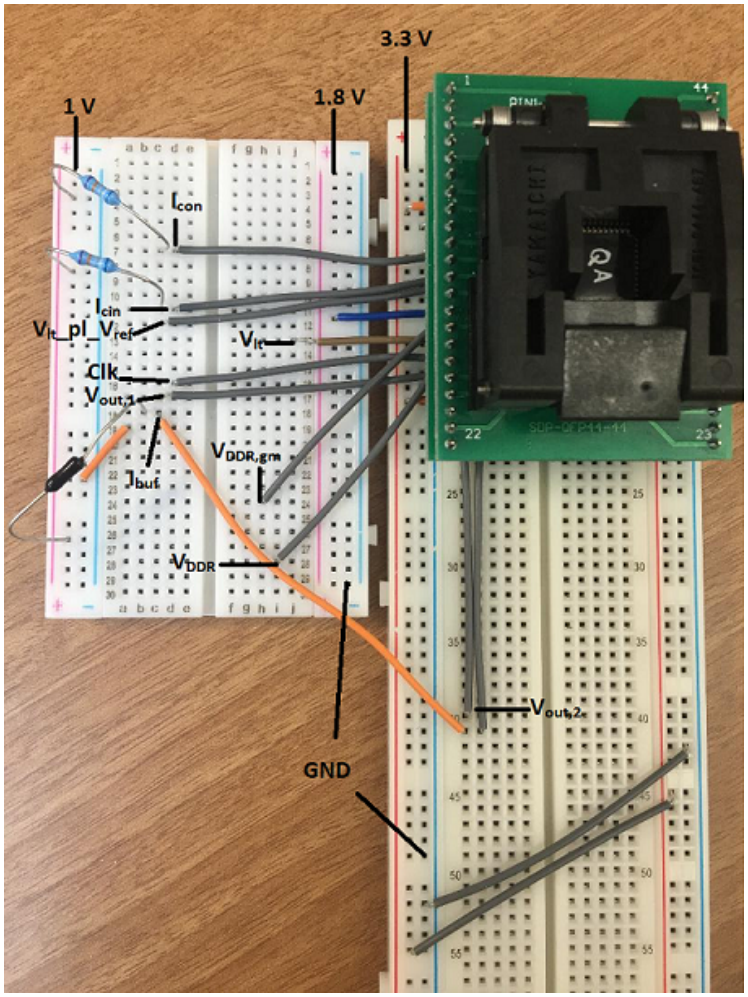

Figure 3.14: Testbench setup.

3.5.2 Test Results

The chip measurements were done using the following equipment:

- Tektronix DPO2012 oscilloscope
- Agilent E3631A power supply
- Agilent 33120a AWG
- P6139B 500 MHz probe

To start, the DC conditions of the chip are checked in the reset state. The reset state is defined as the state where the clock is held at 1.8 V, so all integrating capacitors are discharged. Table 3.6 summarizes the measurements in the reset state.

Measurement	Simulated	Measured
$V_{ddgmref}$	1.41 V	1.44 V
V_{REF}	1.387 V	1.369 V
$V_{out,1}$	0.699 V	0.698 V
$V_{out,2}$	0.699 V	0.711 V
I_{con}	.8855 uA	.888 uA
I_{cin}	1.008 uA	1.019 uA
I_{outbuf}	9.358 uA	8.38 uA
DC @ I_{con}	.3819 V	.3766 V
DC @ I_{cin}	.2961 V	.2913 V
DC @ I_{outbuf}	.5321 V	.567 V

Table 3.6: Reset state measurements. The DC voltage is measured at both voltage input pins and current input pins.

After it was determined from the reset state testing that there are no obvious issues with the testbench nor the chip, the exponential pulse can be measured. The AWG is set to generate a 205 kHz, 80% duty cycle square wave toggling from 0 V to 1.8 V. Figure 3.14 below shows a oscilloscope shot of $V_{out,1}$.

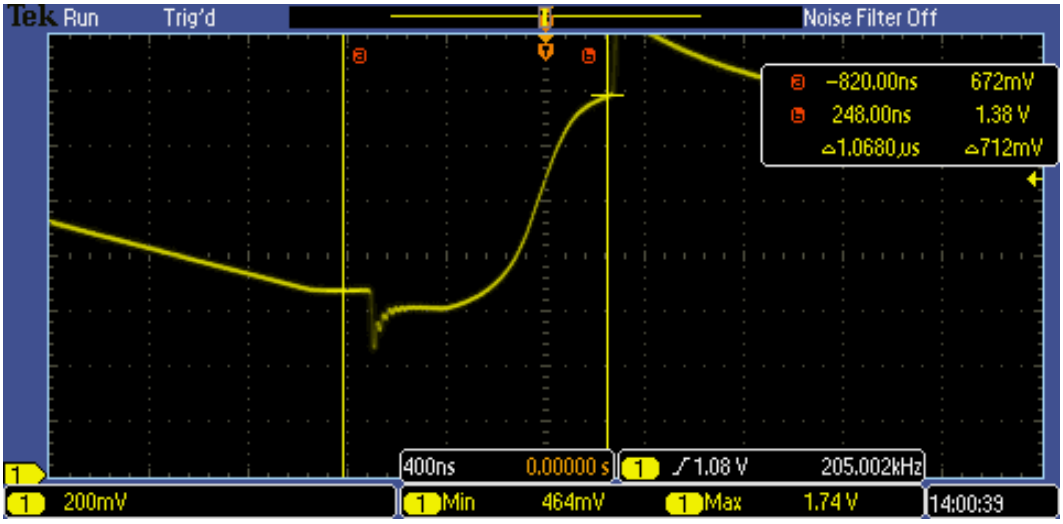

Figure 3.15: Measured pulse.

In this scope picture, we find that the exponential pulse begins with a negative jump in magnitude, as predicted by the analysis in chapter 2. It rises to a maximum value of around 1.38 V, at which point it starts to saturate. At this point, the clock rises and the discharge cycle begins, eventually settling to a DC voltage of 0.672 V.

3.5.3 Comparison With Simulation

From figure 3.15 we see that the oscilloscope shot is divided into a grid of dotted rectangles that are each 400 ns wide and 200 mV tall. From this we get a close estimate of the time it takes for the pulse to rise to its peak before saturating, which is approximately 650 ns. This is larger than the 500 ns it

takes in simulation at the TT corner. One possible explanation is that the chip was fabricated at a slower corner, which causes the pulse to rise more slowly.

Another point of comparison is the discharge time. From the simulation, we see that the discharge time is close to 200 ns. However, the measured result is several times longer. This because there is a very large capacitance seen at the output pin, resulting from the breadboard, package, and probe parasitics. The combination of these parasitic capacitances is much larger than the 5pF used in the simulation.

Lastly, there is a much more pronounced jump in voltage at both the start and the end of the measured pulse. A combination of effects due to abrupt switching, charge injection, and non-idealites in the packaging/testbench may give rise to to these glitches. As no packaging effects were considered in the simulation, this may be a big contributing factor to this discrepancy.

Chapter 4

Exponential Pulse Generator: Second Design

This chapter presents a much faster version of the same circuit presented in the previous chapter. The overall architecture is the same, with the main differences being device sizing and using a cascoded current mirror as opposed to a non-cascoded mirror.

4.1 Differences Summarized

4.1.1 Device Sizing

The device sizing of each circuit block is presented in tables 4.1 and 4.2. The key difference is the use of minimum channel length devices in the integrator to get a much higher g_m. As explained in chapter 2, a higher g_m leads to a more ideal integrator.

Device	Size (μm)
M_1	20/0.18
M_2	360/0.25
M_3	1/0.25

Device	Size (μm)
M_1	20/0.18
M_2	252/0.25
M_3	1/0.25

Table 4.1: Device sizings. (left) V_{DDR} generating circuit, fig. 3.1 (right) $V_{DDR,gm}$ generating circuit, fig. 3.2.

Device	Size (μm)
Integ. NMOS	7.5/0.18
Integ. PMOS	17.5/0.18
g_m NMOS	1.5/0.18
g_m PMOS	3.5/0.18

Device	Size
NMOS	12/0.3
PMOS	24/0.3

Device	Size
$M_{0,b}$	7/3
$M_{0,a}$	1.4/3
M_1 - M_{2k+2}	7/3

Table 4.2: (left) Sizings for integrator/g_m inverters, fig 3.3a. (center) Sizings for switch devices, fig 3.3b. (right) Sizings for current mirror devices, presented in the next section.

4.1.2 Current Mirror

An improved current mirror for supplying the integrating current is also designed. The previous version did not use cascoding, which limits output impedance. A cascoded current mirror allows for a much higher output impedance, at the cost of decreased headroom. To partially alleviate the headroom issue, a low voltage cascoded structure is used. This configuration allows a voltage of about one V_{th} lower at the drain of the cascode devices, as compared to the traditional cascoded current mirror [1]. Devices $M_{0,a}$ and $M_{0,b}$ are used

to generate an adequate bias voltage for the cascoded devices. A mirror ratio of 1:1 is used to maintain high accuracy in the current mirroring. Figure 4.1 shows the implementation of this current mirror.

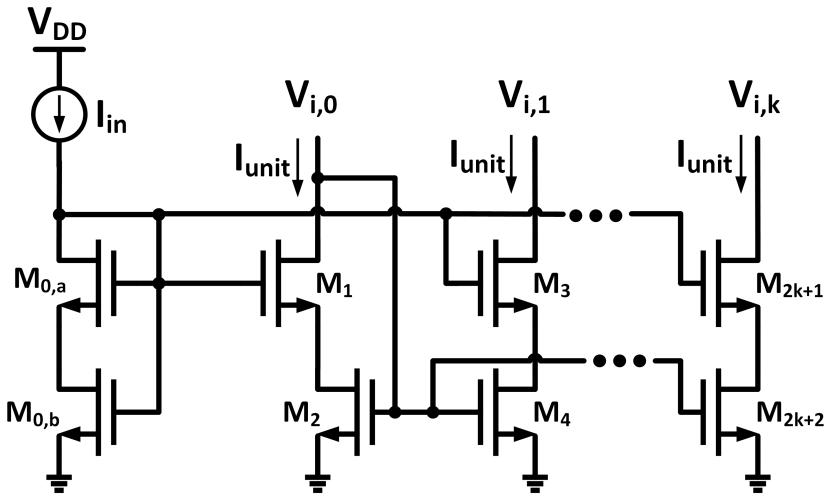

Figure 4.1: Low voltage cascoded current mirror.

4.2 Simulation Results

In this section, we discuss all simulation results for the new exponential pulse generator. This design achieves a time constant $\tau = 0.4$ ns, as opposed to the previous design of $\tau = 100$ ns. Similar to the previous chapter, we consider the effects of PVT on the exponential pulse, as well as their effect on the regulated voltages. There is no layout done for the circuit blocks presented in this section.

4.2.1 Integrator Outputs

First, we present the simulated results taken at each integrator output. The expectation is that the output of the first integrator rises linearly, the second quadratically, etc. This is confirmed in figure 4.2, where the outputs follow the expectation quite closely. This simulation was done at T=27°C, TT corner, and $V_{DD} = 1.8$ V.

There are a few things to note in this plot. First, the difference between the first and second stage outputs is quite large, while the difference between the fourth and fifth stage output is relatively small. This is because each additional term in the exponential function's power series contributes much less than the term before it. Secondly, the clock duty cycle was chosen so that the fifth stage output is reset when it reaches around 1.2 V, preventing the PMOS device in the integrator from going to triode region.

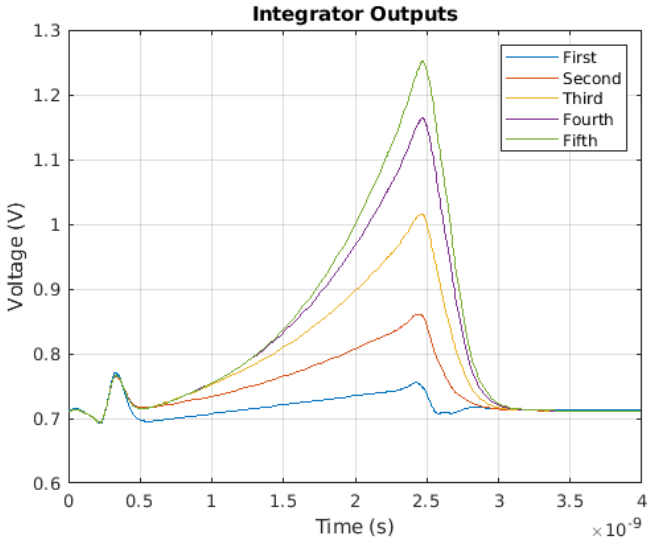

Figure 4.2: Integrator outputs at normal PVT.

Another way to understand the difference between successive curves is to cal-

culate the area underneath, and normalizing to the area underneath the first term output. First, every curve is truncated to [600ns 2.5ns], which is the period of time when the integration occurs. Table 4.3 lists the different outputs and their corresponding normalized area. As shown, there is over 100% difference between the first two areas, but only a 10% difference between the fourth and the fifth.

Output Number	Normalized Area
1^{st}	1
2^{nd}	2.3553
3^{rd}	3.767
4^{th}	4.7688
5^{th}	5.24746

Table 4.3: Outputs curves and their normalized areas.

4.2.2 Outputs Over PVT

To understand how the circuit varies over PVT, simulation is done over a variety of corners (TT,SS,FF,SF,FS), temperatures (0°C, 27°C, 100°C), and supply voltages (1.62 V, 1.8 V, 1.98 V). First, we plot the exponential pulse by varying two of the three parameters, and keeping the last one fixed. Then, we will also discuss the impact of PVT variations on the regulated voltages, V_{DDR} and $V_{DDR,gm}$. Figure 4.3 below shows the exponential pulse at different PVT. The regulated voltages at normal temperature and V_{DD} are plotted in figure 4.4. Figures 4.5 and 4.6 show the variation in the regulated voltages due to PVT.

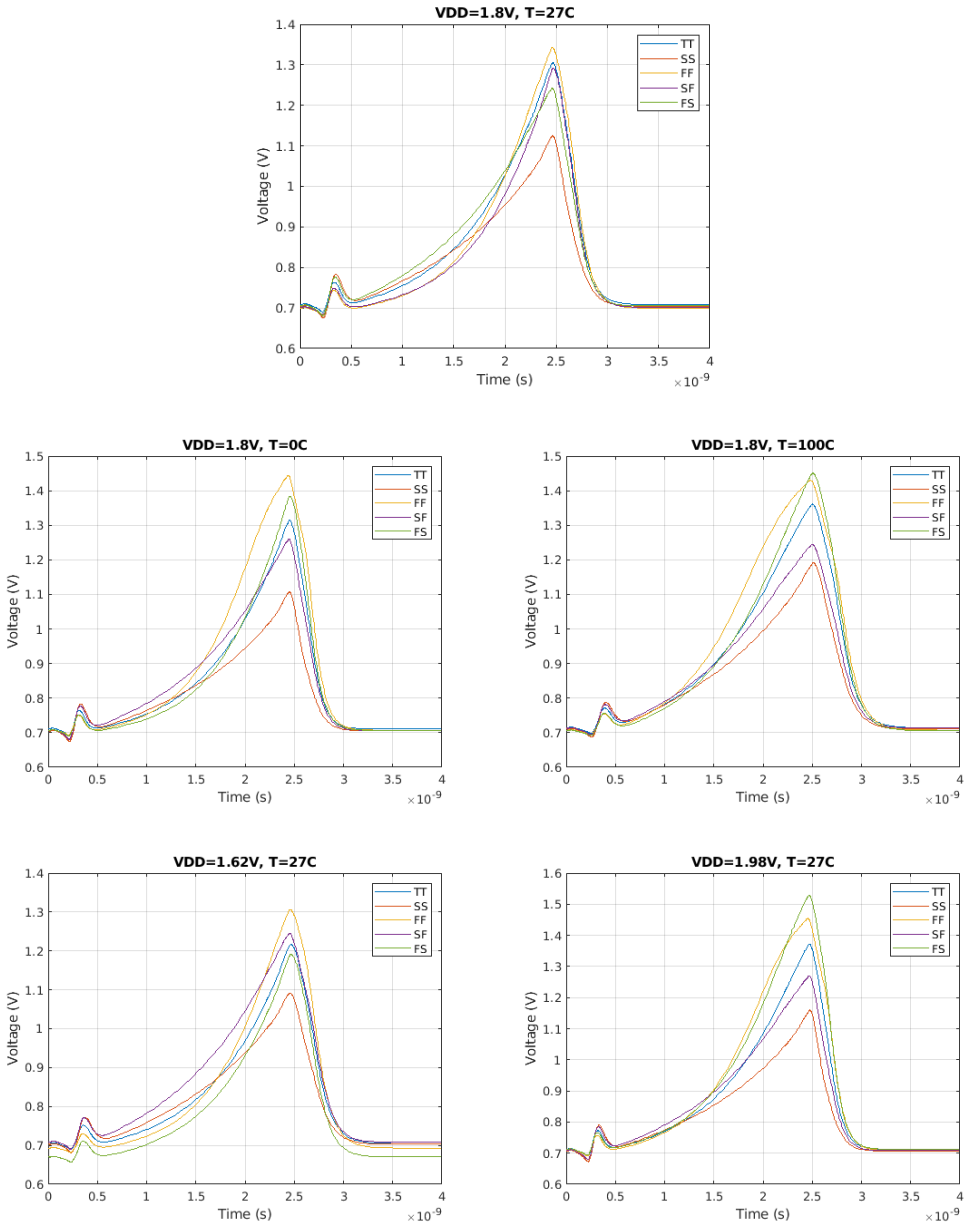

Figure 4.3: Variations in the exponential pulse due to PVT. The top center plot is at typical temperature and typical supply voltage.

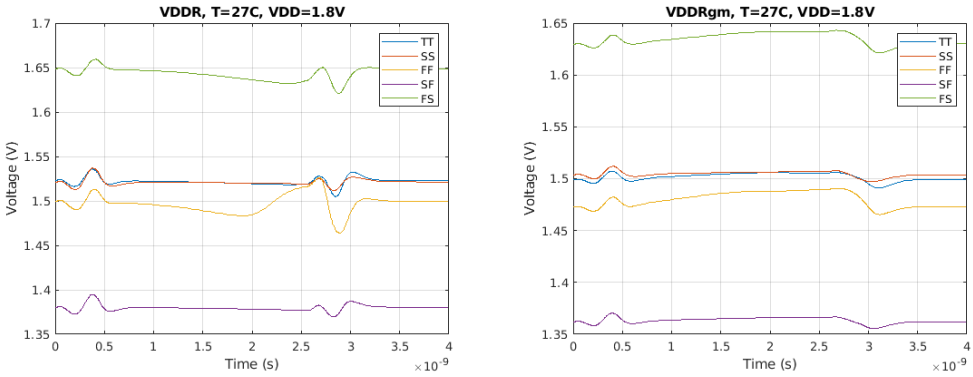

Figure 4.4: Regulated voltages at normal temperature and V_{DD}.

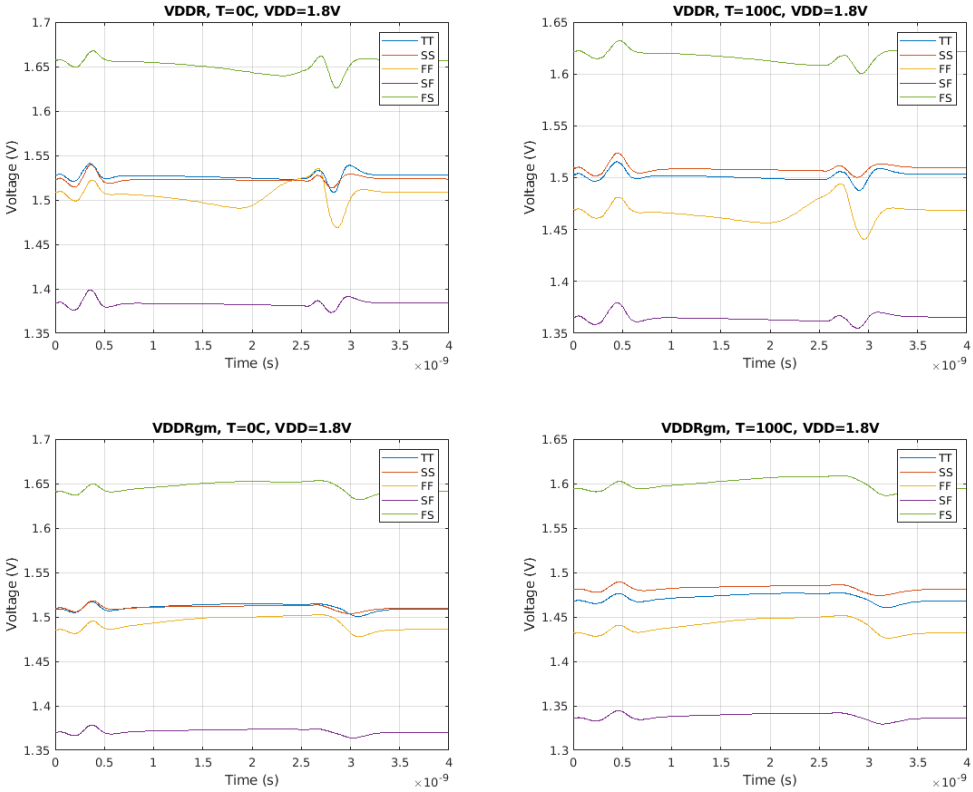

Figure 4.5: Effects of temperature variation on V_{DDR} and $V_{DDR,gm}$.

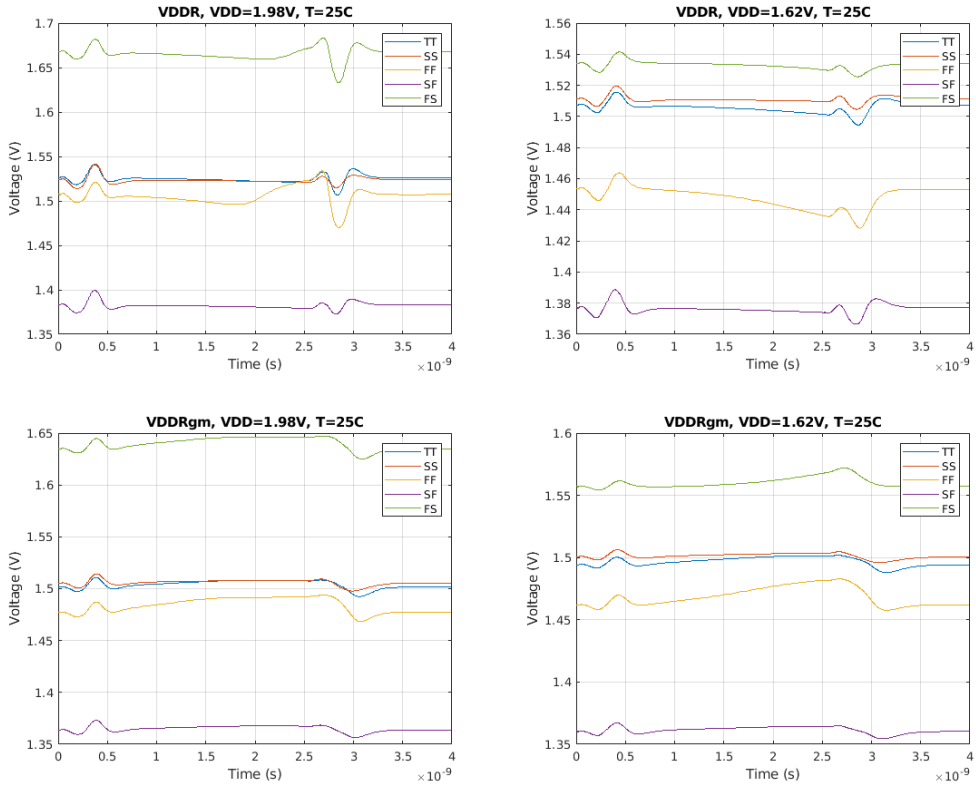

Figure 4.6: Effects of supply voltage variation on V_{DDR} and $V_{DDR,gm}$.

From figure 4.3 we can determine that the two extremes are at the SS and FF corners. In the SS corner, the pulse rises slowly, due to the decreased mobility of both NMOS and PMOS devices. This then affects the time constant of integration. Similarly, mobility is higher in the FF corner. This causes the pulse to rise much faster compared to the typical case. There is minimal variation in the pulse due to temperature variation. As shown, the plots at 0°C and 100°C do not vary much when compared to the typical temperature case. At high V_{DD}, the plot is very similar to that of the typical plot. This is because the regulated supply voltages stay relatively constant, and so the inverters do not see the higher V_{DD}. However, if V_{DD} goes lower, then there will be issues

caused by the reduced headroom. This is evident in the bottom right graph of figure 3.6, where the peak voltage reached by the pulse is much lower than that of the other cases.

Figure 4.5 shows the effect of temperature variation on different corners of the regulated supply voltages. With the exception of the FF corner, V_{DDR} remains fairly constant across the entire integration period. The reason why the FF corner sees a spike near the end is because the exponential pulse starts to saturate, driving the PMOS of the inverter into triode. This causes the sudden bump near the 2.5 ns mark. As the corners change, V_{DDR} is also adjusted to keep V_{LT} relatively constant. This is evident from figure 4.3, where all pulses start at nearly the same voltage, no matter the corner.

Similarly, figure 4.6 shows the effect of supply voltage variation on different corners of the regulated voltages. The worst case scenario is when V_{DD} drops to a lower value, which results in decreased headroom. This cases the most significant difference when compared to the typical case. At high V_{DD}, the graphs for both V_{DDR} and $V_{DDR,gm}$ match more closely to that of the typical case.

Chapter 5

Conclusion

In this thesis, we present a new way of generating an exponential pulse using CMOS inverters. In chapter 2, we describe the method of using integrators to generate an exponential pulse. Additionally, we describe how an inverter-based integrator works, and compare it to a more traditional opamp-based integrator. In chapter 3, we present a first design of the exponential pulse generator circuit. Since inverters are particularly prone to PVT variations, we also designed some circuits for reducing the impact of these variations on critical parameters. Then, the layout of each block is given, along with post-layout simulations. Finally, measurements were done on a chip. Chapter 4 describes a second version of the same exponential pulse generator. This version was designed to be much faster than the previous version, achieving a time constant on the order of nanoseconds, as opposed to microseconds.

There are several ways to extend the work in this thesis. One immediate step would be to tape out the second design, and verify the results in the lab. Improvements to the testbench can be made, where a PCB is used instead of a breadboard. Once a chip is verified, we could test the accuracy of the pulse

with real cables, and see how it compares to conventional methods. Finally, it would be interesting to see if this idea could be extended to measuring distances for applications such as autonomous vehicles, where accuracy is of high importance.

Bibliography

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Boston, 2001.

[2] Cheng-Chieh Chang and Shen-luan Liu, "Current-mode pseudo-exponential circuit with tunable input range," in *Electronic Letters*, vol. 36, no. 16, pp 1335-1336, 3 Aug. 2000.

[3] Conley, Tim (2003), "The relationship among component age, usage (reliability) and cost of naval aviation repairables", *Aging Aircraft Conference* 2003, New Orleans, Sept.

[4] F. Shoucair, "Design Consideration in High Temperature Analog CMOS Integrated Circuits," in *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 9, no. 3, pp. 242-251, September 1986.

[5] Furse, C., Chung, Y.C., Lo, C., and Pendayala, P. A Critical Comparison of Reflectometry Methods for Location of Wiring Faults, Journal of Smart Structures and Systems, 2(1), 2006, pp. 25-46.

[6] G. Palmisano and R. Salerno, "A replica biasing for constant-gain CMOS open-loop amplifiers," 1998 *IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterey, CA, 1998, pp. 363-366 vol.2.

[7] J. Bastos et al., "Mismatch characterization of small size MOS transistors," *Proceedings International Conference on Microelectronic Test Structures*, Nara, Japan, 1995, pp. 271-276.

[8] J. R. Andrews, "Time Domain Reflectometry (TDR) and Time Domain Transission (TDT) Measurement Fundamentals", Precision Pulse Labs Application Note AN-15, November 2004.

[9] J. W. Fattaruso, "Low-voltage analog CMOS circuit techniques," *1999 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers. (Cat. No.99TH8453)*, Taipei, Taiwan, 1999, pp. 286-289.

[10] K. R. Lakshmikumar, R. A. Hadaway and M. A. Copeland, "Characterisation and modeling of mismatch in MOS transistors for precision analog design," in *IEEE Journal of Solid-State Circuits*, vol. 21, no. 6, pp. 1057-1066, Dec. 1986.

[11] K. R. Raghunandan and T. R. Viswanathan, "CMOS inverter-based voltage and current references in short channel technologies," *2014 IEEE Dallas Circuits and Systems Conference (DCAS)*, Richardson, TX, 2014, pp. 1-4.

[12] M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching properties of MOS transistors," in *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433-1439, Oct. 1989.

[13] M. K. Ash, R. H. Flake and T. R. Viswanathan, "Exponential pulse generator for a time domain reflectometer," *2015 IEEE Dallas Circuits and Systems Conference (DCAS)*, Dallas, TX, 2015, pp. 1-4.

[14] M. K. Smail, L. Pichon, M. Olivas, F. Auzanneau and M. Lambert, "Detection of Defects in Wiring Networks Using Time Domain Reflectometry," in *IEEE Transactions on Magnetics*, vol. 46, no. 8, pp. 2998-3001, Aug. 2010.

[15] P. Kinget, S. Chatterjee and Y. Tsividis, "Ultra-Low Voltage Analog Design Techniques for Nanoscale CMOS Technologies," *2005 IEEE Conference on Electron Devices and Solid-State Circuits*, Howloon, Hong Kong, 2005, pp. 9-14.

[16] Raghunandan, Kolar Ranganathan, " Structured analog design in deep sub-micron technologies using CMOS inverters and current mirrors," Ph.D dissertation, Cockrell School of Eng., The Univ. of Texas at Austin, Austin, 2017. Accessed on Feb. 2, 2020. [Online]. Available: https://repositories.lib.utexas.edu/handle/2152/63492

[17] R. Stata "Operational integrators" Analog Dialogue vol. 1 no. 1 Apr. 1967.

[18] Weste, Neil H.E. & Harris, David (2005). *CMOS VLSI Design: A Circuits and Systems Perspective, 3rd Ed.*,. Addison-Wesley, pp.231-235. ISBN 0-321-14901-7.